ABSTRACT OF THE DISCLOSURE

An SZ (size information) section is provided for each of registers that make up a register file. Suppose an instruction decoded requests that operand data of a particular size be loaded from a RAM into the register file or that immediate operand data of a particular size be transferred to the register file. Then, the size information of the operand data will be retained in the SZ section. The instruction decoded may also be an arithmetic and logical operation instruction requesting that operand data in the register file be referred to or an instruction requesting that the operand data be stored from the register file into the RAM. In such a case, the size information will be read out from the SZ section of the register file and only parts of various components constituting manipulation means (like ALU), which have been specified by the size information, will be enabled. As a result, the power, which is usually dissipated by a processor handling data of multiple sizes, can be cut down effectively.